a memory cell composed of the ferroelectric capacitor and the memory cell transistor; and

dummy bit lines connected to the ferroelectric capacitor that is not used for the circuit operation,

C1

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode;

wherein the memory cell comprises a memory cell array arranged in a matrix, and

wherein the dummy bit line is arranged at the edge of the memory cell array.

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8. (Amended) A ferroelectric memory device comprising:

Sub D3

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

C2

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film;

a second inteconnection layer formed on the upper interlevel dielectric film,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode; and

wherein the second interconnection layer totally covers the top electrode of the ferroelectric capacitor in the planar layout.